ABSTRACT OF THE DISCLOSURE

A timing recovery loop in the front end of a digital receiver includes a sample rate converter which receives a symbol stream at a first sampling rate and outputs the symbol stream at a second sampling rate responsive to a timing recovery (TR) control signal, a forward equalizer generating an equalized feedback signal based on the symbol stream at the second sampling rate, and a timing recovery circuit generating the TR control signal based upon the equalized feedback signal. If desired, the timing recovery loop may include a carrier recovery circuit electrically coupling the sample rate converter to the forward equalizer and a finite impulse response (FIR) filter electrically coupling the carrier recovery circuit to the forward equalizer. In an exemplary case, the FIR filter is a square-root raised cosine filter. A method for controlling the timing recovery loop based on the equalized feedback signal and a corresponding timing recovery control signal are also described.